Single Chip TV Baseband Processor

Description

The U4930B is an alignment-free, I^2C-bus controlled TV baseband processor that has been designed for use with the baseband delay line U3665M and the SECAM decoder U4935B.

The IC includes a multiple video-input selector switch, chroma filters, sharpness control and black level stretcher function, PAL/NTSC color decoder, luminance processor, RGB control, the sync and deflection processor.

The IC is realized in a bipolar VLSI technology and operates with +5/+8 V supply voltage. Easy interfacing and the optional add-on SECAM decoder U4935B provides flexibility to design a multistandard TV.

Features

- Multiple video switch with two CVBS inputs and a SVHS (or third CVBS) input
- CVBS output signals for the teletext decoder and a SCART interface
- Y delay, sharpness control and black level stretcher function in the luminance channel
- Integrated and auto-tuned chroma traps, band pass filters
- PAL/NTSC color decoder with automatic color standard decoder
- Easy interfacing with an add-on SECAM decoder for multistandard applications
- RGB control with cut-off and white point adjustment, linear RGB input and fast blanking
- Synchronization with drive circuits for H/V deflection
- Vertical compression of the picture for 16:9 on 4:3 TV sets
- I^2C-bus control of all functions, no manual alignment
- Minimum number of external components

Ordering Information

Extended Type Number	Package	Remarks
U4930B-A	SDIP52	

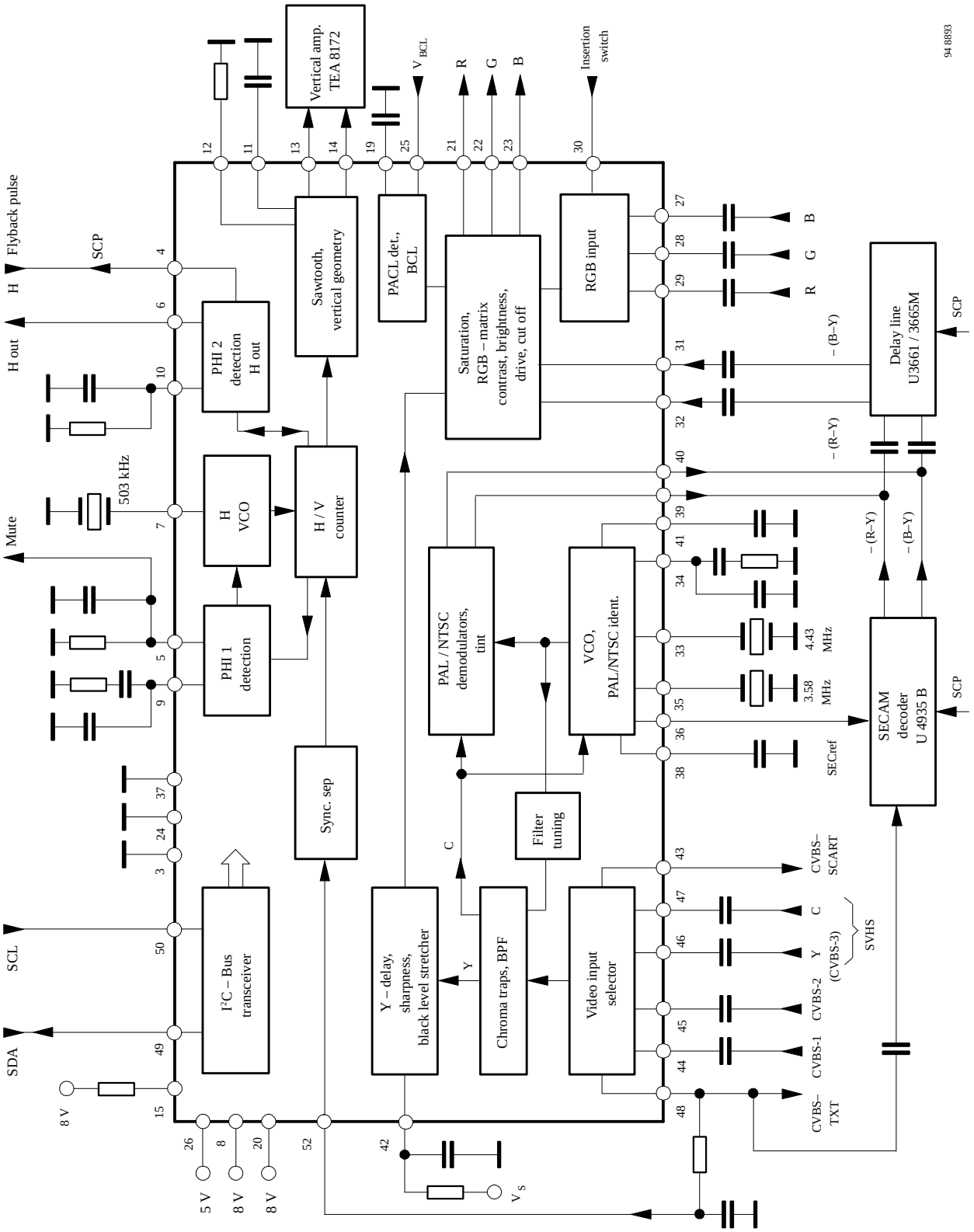


Figure 1. Block diagram

Pin Description

Pin	Symbol	Function
1	NC	Not connected
2	Test	Pin for testing
3	GND	Ground (deflection)
4	SCP	Sandcastle pulse output / H-flyback pulse input
5	Mute	Mute output filter
6	H out	Horizontal output
7	H osc.	Horizontal oscillator (503 kHz)
8	Vs (8 V)	8-V supply voltage (deflection)
9	PHI1	PHI1 loop filter
10	PHI2	PHI2 loop filter
11	C_{Saw}	Vertical sawtooth capacitor
12	I_{ref}	Reference current
13	V drive(+)	Vertical drive (positive)
14	V drive(–)	Vertical drive (negative) / vertical pulse
15	Vs	Supply voltage (digital)
16	NC	Not connected
17	NC	Not connected
18	NC	Not connected
19	ACL	Automatic contrast limiting filter
20	Vs (8 V)	8-V supply voltage (RGB)
21	R out	R output
22	G out	G output
23	B out	B output
24	GND	Ground (RGB)
25	V_{BCL}	Beam current limiter input
26	Vs (5 V)	5-V supply voltage (luminance/chrominance)
27	B in	B input
28	G in	G input
29	R in	R input
30	Insert. sw.	Insertion switch
31	–(B–Y) in	–(B–Y) input
32	–(R–Y) in	–(R–Y) input
33	Xtal1	Crystal 4.43 MHz
34	APC	APC filter
35	Xtal2	Crystal 3.58 MHz
36	SEC_{ref}	SECAM reference output
37	GND	Ground (luminance/chrominance)
38	$C_{freq.}$	Ident filter (frequency)
39	–(R–Y) out	–(R–Y) output
40	–(B–Y) out	–(B–Y) output
41	C_{phase}	Ident filter (PAL phase)
42	C_{BPH}	Black peak hold time constant
43	CVBS–SCART	CVBS-SCART output
44	CVBS–1	CVBS-1 input
45	CVBS–2	CVBS-2 input
46	Y(SVHS)	Y(SVHS) input (or CVBS-3 input)
47	C(SVHS)	C(SVHS) input
48	CVBS–TXT	CVBS-TXT output
49	SDA	SDA (I^2C-bus)
50	SCL	SCL (I^2C-bus)
51	NC	Not connected
52	Sync	Sync separator input

Pin Connection Diagram

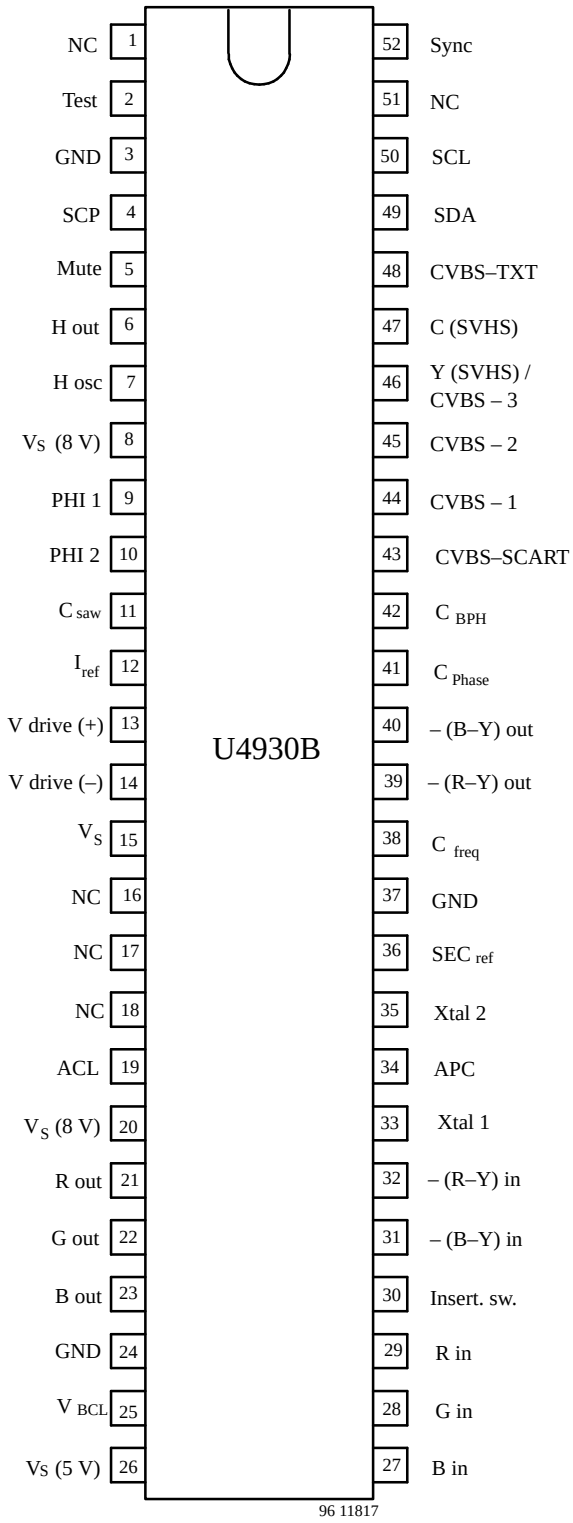


Figure 2. Pin connection diagram

I²C–Bus Specification

The I²C-bus is a bi-directional, two-wire bus for inter-communication between the microcontroller and the IC. The transmission is done over a serial data line (SDA) and synchronized by a serial clock line (SCL). Both lines are LOW activ.

Each transmission must begin with a start condition and end with a stop condition. Between a start and a stop condition, when SCL is HIGH, the data line SDA must be stable. Only while SCL is LOW is the data line allowed to change. Each transmission consists of at least three bytes. Each byte has to be followed immediately by an acknowledge bit “A”.

The maximum clock frequency is 100 kHz.

TTL level (HIGH > 3 V, LOW < 1.5 V) is used for driving.

The module address for the U4930B is “BA”$_{hex}$ or “1011 1010”$_2$ in the write mode.

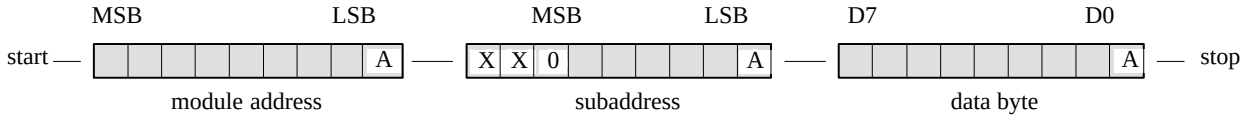
The IC differentiates between normal and autoincrement mode transmission. For the autoincrement mode, set the sixth bit of the subaddress byte to “1”.

In the autoincrement mode, the subaddress can be followed by more than one byte. The bytes from the third byte on will all be interpreted as data. The subaddress will be internally automatically incremented and the IC stores the data successively in the correct registers.

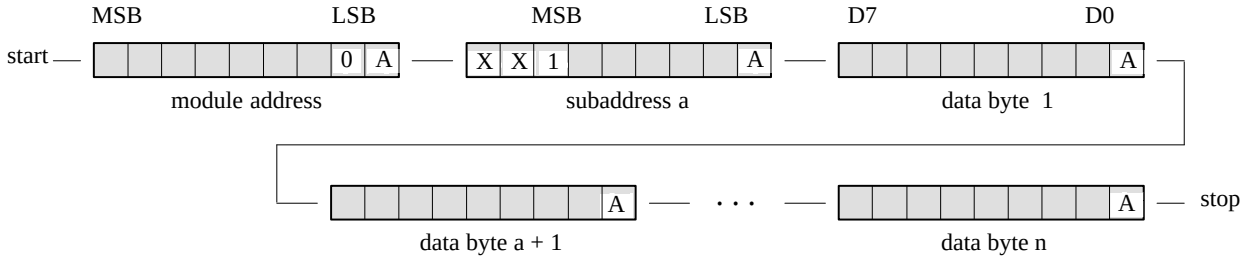
By programming the read/write bit “1” – LSB in the module address byte – the IC provides information about its internal status. When POD is read out for the first time, this bit is “1”. All other read out result in “0” until the next power down / up process occurs.

Write mode (module address is “1011 1010”$_{2)}$:

1. Normal mode



2. Autoincrement mode



Read mode (module address is “1011 1011”$_{2)}$:

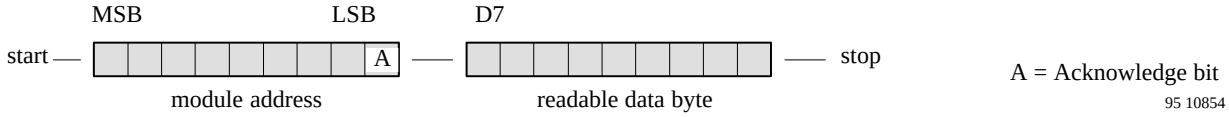


Figure 3. I²C-bus transmission modes of the U4930B

Subaddress and Data Bytes

Register		Sub–address (hex)	Data Byte							
			D7	D6	D5	D4	D3	D2	D1	D0
1.	Brightness *)	00	x	BRI6	BRI5	BRI4	BRI3	BRI2	BRI1	BRI0
2.	Contrast *)	01	x	CON6	CON5	CON4	CON3	CON2	CON1	CON0
3.	Tint *)	02	x	TIN6	TIN5	TIN4	TIN3	TIN2	TIN1	TIN0
4.	Saturation *)	03	x	SAT6	SAT5	SAT4	SAT3	SAT2	SAT1	SAT0
5.	Sharpness *)	04	x	x	SH5	SH4	SH3	SH2	SH1	SH0
6.	R – drive	05	x	x	RDR5	RDR4	RDR3	RDR2	RDR1	RDR0
7.	B – drive	06	x	x	BDR5	BDR4	BDR3	BDR2	BDR1	BDR0
8.	R – cut off	07	RCO7	RCO6	RCO5	RCO4	RCO3	RCO2	RCO1	RCO0
9.	G – cut off	08	GCO7	GCO6	GCO5	GCO4	GCO3	GCO2	GCO1	GCO0
10.	B – cut off	09	BCO7	BCO6	BCO5	BCO4	BCO3	BCO2	BCO1	BCO0
11.	VideoSW1	0A	x	TRP1	TRP0	TRPD	AUTO	3.58	NTSC	SEC
12.	VideoSW2	0B	x	YDL1	YDL0	YDLS	ISB1	ISB0	ISA1	ISA0
13.	VideoSW3	0C	x	x	x	BPFC	BPFD	VMUT	BLS	PACL
14.	H – shift	0D	x	x	HSH5	HSH4	HSH3	HSH2	HSH1	HSH0
15.	V – slope	0E	x	x	VSL5	VSL4	VSL3	VSL2	VSL1	VSL0
16.	V – size	0F	x	COMP	VSZ5	VSZ4	VSZ3	VSZ2	VSZ1	VSZ0
17.	S – correction	10	x	x	SCO5	SCO4	SCO3	SCO2	SCO1	SCO0
18.	V – shift	11	x	x	VSH5	VSH4	VSH3	VSH2	VSH1	VSH0
19.	DeflectionSW	12	x	FFB	FFA	VDSM	PH1T	HPD	SERV	VPE

Readable Data Byte							
60HZ	MUTE	n.u.	POD	3.58	NTSC	SEC	STID

x = Don’t care

*) = Will be executed during the vertical fly-back time

n.u. = not used

Data Byte Input Conditions

Function	Bitname	Input Conditions				Initial and Nominal Settings
Forced color standard select	SEC, NTSC, 3.58	3.58	NTSC	SEC	Color standard	PAL – 4.43
		0	0	0	PAL – 4.43	
		1	0	0	PAL – 3.58	
		1	1	0	NTSC – 3.58	
		0	1	0	NTSC – 4.43	
		0	0	1	SECAM	
Auto mode	AUTO	0 = forced color standard 1 = automatic search for the color standard				Forced
Trap switch disabled	TRPD	0 = chroma trap ON 1 = chroma trap OFF				ON
Trap select	TRP0, TRP1	TRP1	TRP0	trap for		PAL/NTSC
		0	0	SECAM		
		1	1	PAL/NTSC		
CVBS-TXT switch	ISA0, ISA1	ISA1	ISA0	CVBS-TXT/ decoder output		CVBS-1
		0	0	CVBS–1		
		0	1	CVBS–2		
		1	0	Y(SVHS) + C(SVHS)		
		1	1	CVBS-3		
CVBS-SCART switch	ISB0, ISB1	ISB1	ISB0	CVBS–SCART output		CVBS-1
		0	0	CVBS–1		
		0	1	CVBS–2		
		1	0	Y(SVHS) + C(SVHS)		
		1	1	CVBS–3		
Y – delay	YDLS, YDL0, YDL1	YDL1	YDL0	YDLS	Delay time (ns)	240 ns
		0	1	1	90	
		0	1	0	120	
		1	0	1	180	
		1	0	0	240	
		1	1	1	300	
		1	1	0	360	

Data Byte Input Conditions (continued)

Function	Bitname	Input Conditions	Initial and Nominal Settings
Peak ACL	PACL	0 = peak ACL detection at 120 IRE 1 = peak ACL detection at 150 IRE	150 IRE
Black-level stretcher	BLS	0 = black level stretcher OFF 1 = black level stretcher ON	OFF
Video mute switch	VMUT	0 = video mute OFF 1 = video mute ON	OFF
Band pass filter disable	BPFD	0 = chroma band pass filter ON 1 = chroma band pass filter OFF	ON
Band pass filter correction	BPFC	0 = chroma band pass filter correction ON 1 = chroma band pass filter correction OFF	OFF
Compressed mode	COMP	0 = V – size normal 1 = V – size compressed	Normal
Vertical pulse enable	VPE	0 = vertical sawtooth 1 = vertical pulse	Vert. sawtooth
Service switch	SERV	0 = vertical deflection ON 1 = vertical deflection OFF (service mode)	ON
Horizontal pulse enable	HPD	0 = horizontal pulse enabled 1 = horizontal pulse disabled	Enabled
PHI1 time constant	PH1T	0 = PHI1 time constant FAST 1 = PHI1 time constant SLOW (during vertical retrace FAST)	FAST
Vertical divider	VDSM	0 = normal operation of the vertical divider 1 = vertical divider switched to search mode valid only for PHI1 loop locked	Normal
Forced field frequency	FFB, FFA	FFB | FFA | 0 | 0 | search 0 | 1 | forced 60 Hz 1 | 0 | forced 50 Hz valid only for PHI1 loop not locked	Search

Readable Status Bits

Function	Bitname	Input Conditions			
Search mode indication	STID	0 = search mode active 1 = color standard identified			
Color standard decoder mode	SEC, NTSC, 3.58	3.58	NTSC	SEC	Color standard
		0	0	0	PAL – 4.43
		1	0	0	PAL – 3.58
		1	1	0	NTSC – 3.58
		0	1	0	NTSC – 4.43
		0	0	1	SECAM
Power down indication	POD	0 = normal mode 1 = power down occured since last reading			
PHI1 lock indication	MUTE	0 = PHI1 loop locked 1 = PHI1 loop not locked (mute)			
Field frequency indication	60HZ	0 = field frequency ≠ 60 Hz 1 = field frequency 60 Hz			

Nominal Settings

	Register	Subaddress (hex)	Control Range	Nominal Settings
1.	Brightness	00	0 to 127	71
2.	Contrast	01	0 to 127	58
3.	Tint	02	0 to 127	64
4.	Saturation	03	0 to 127	72
5.	Sharpness	04	0 to 63	16
6.	R – drive	05	0 to 63	30
7.	B – drive	06	0 to 63	30
8.	R – cut off	07	0 to 255	128
9.	G – cut off	08	0 to 255	128
10.	B – cut off	09	0 to 255	128
14.	H – shift	0D	0 to 63	32
15.	V – slope	0E	0 to 63	32
16.	V – size	0F	0 to 63	32
17.	S – correction	10	0 to 63	32
18.	V – shift	11	0 to 63	32

Absolute Maximum Ratings

Reference point Pins 3, 24 and 37, unless otherwise specified

Parameters	Symbol	Pin	Value	Unit
Supply voltage	V_S	8, 20 26	9.0 5.5	V V
Output currents	I_{out}	6	5	mA
Junction temperature	T_j		+150	°C
Storage temperature range	T_{stg}		–25 to +150	°C
Electrostatic handling *)	V_{ESD}	All pins	±200	V

*) Equivalent to discharging a 200 pF capacitor via a 0-Ω resistor

Operating Range

Parameters	Symbol	Pin	Value	Unit
Supply voltage range	V_S	8, 20 26	7.6 to 8.4 4.75 to 5.25	V V
Ambient temperature	T_{amb}		0 to +70	°C

Thermal Resistance

Parameters	Symbol	Test Condition	Value	Unit
Junction ambient	R_{thJA}	When soldered to PCB	40	K/W

Electrical Characteristics

V_S = 5 V/ 8 V, T_{amb} = 25°C; reference point Pins 3, 24 and 37, unless otherwise specified
Test conditions: nominal settings (see tables on pages 7, 8 and 9), CVBS-1 = 1 V (peak-to-peak value), unless otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
DC supply						
Supply voltage	Pin 8 Pin 20 Pin 26	V_s		8 8 5		V V V
Supply current	Pin 8 Pin 20 Pin 26	I_s		25 20 65		mA mA mA
I^2C bus						
Input voltage for HIGH level	Pins 49, 50	V_{iH}	3.0			V
Input voltage for LOW level	Pins 49, 50	V_{iL}			1.5	V
Input current	Pins 49, 50	I_i			1	A
Output voltage for LOW level	Isink = 3 mA, Pin 49	V_{oL}			0.4	V
Power down reset threshold level	Pin 8	V_s		4		V
Video input selector – Inputs						
CVBS-1 input signal (peak-to-peak value)	Pin 44	v_{44}		1.0	1.4	V
CVBS-1 clamping level	Pin 44	V_{44}		2.1		V
CVBS-1 input impedance	Input voltage over clamping level Pin 44	Z44	1			MΩ
CVBS-2 input signal (peak-to-peak value)	Pin 45	v_{45}		1.0	1.4	V
CVBS-2 clamping level	Pin 45	V_{45}		2.1		V
CVBS-2 input impedance	Input voltage over clamping level Pin 45	Z_{45}	1			MΩ
Y(SVHS) or CVBS-3 input signal (peak-to-peak value)	Pin 46	v_{46}		1.0	1.4	V
Y(SVHS) or CVBS-3 clamping level	Pin 46	V_{46}		2.1		V
Y(SVHS) or CVBS-3 input impedance	Input voltage over clamping level Pin 46	Z_{46}	1			MΩ
C(SVHS) input signal (burst amplitude) (peak-to-peak value)	Chroma/ burst ratio = 2.2/1 Pin 47	v_{47}		0.3	0.42	V
C(SVHS) dc level	Pin 47	V_{47}		2.3		V
C(SVHS) input impedance	Pin 47	Z_{47}		40		kΩ

Electrical Characteristics (continued)

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Video input selector – Outputs						
CVBS-SCART output signal (peak-to-peak value)	Pin 43	v_{43}	0.8	1.0	1.2	V
CVBS-SCART black level	Pin 43	V_{43}		2.4		V
CVBS-SCART output frequency characteristic	3 dB bandwidth Pin 43	f_{BW}		10		MHz
CVBS-SCART output impedance	Pin 43	Z_{43}			250	
CVBS-TXT output signal (peak-to-peak value)	Pin 48	v_{48}	1.6	2.0	2.4	V
CVBS-TXT black level	Pin 48	V_{48}		2.5		V
CVBS-TXT output frequency characteristic	3 dB bandwidth Pin 48	f_{BW}		7		MHz
CVBS-TXT output impedance	Pin 48	Z_{48}			250	
Video input selector						
Attenuation of non selected CVBS-input signal	Pins 43, 48	G_{att}	50			dB
Luminance processing						
Chroma trap filter frequencies – PAL / NTSC – SECAM (combined trap filter)		f		 fsc 4.25 4.406		 MHz
Color subcarrier suppression at trap frequencies	All standards	G_{att}	20			dB
Y delay time min.		t_{dmin}		90		ns
Y delay time max.		t_{dmax}		360		ns
Sharpness control curve	See figure 4					
Sharpness center frequency		f		2		MHz
RGB output level difference between BLS on and BLS off	Black-peak level of the luminance signal at 30 IRE on CVBS-1 Pins 21, 22, 23	V_o	–400	–300	–200	mV
RGB output level difference between BLS on and BLS off	Black-peak level of the luminance signal at 70 IRE on CVBS-1 Pins 21, 22, 23	V_o	–100	0	+100	mV
RGB output level ratio between VMUTE on and VMUTE off	CVBS-1 5 MHz signal (note 1) Pins 21, 22, 23			–40		dB

Electrical Characteristics (continued)

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Chrominance processing – Outputs						
–(R–Y) output signal amplitude (peak-to-peak value)	C (SVHS) 0.3 V (peak-to-peak level) burst amplitude Pin 39	v_{39}		0.53		V
–(R–Y) black level	Pin 39	V_{39}		2.4		V
–(R–Y) output frequency characteristic	3 dB bandwidth Pin 39	f_{BW}	0.8			MHz
–(R–Y) output impedance	Pin 39	Z_{39}		100		Ω
–(B–Y) output signal amplitude (peak-to-peak value)	C (SVHS) 0.3 V (peak-to-peak level) burst amplitude Pin 40	v_{40}		0.67		V
–(B–Y) black level	Pin 40	V_{40}		2.4		V
–(B–Y) output frequency characteristic	3 dB bandwidth Pin 40	f_{BW}	0.8			MHz
–(B–Y) output impedance	Pin 40	Z_{40}		100		
SECAM reference output signal amplitude (peak-to-peak value)	During vertical blanking Pin 36	v_{36}		0.3		V
SECAM reference output dc voltage	PAL/NTSC forced or identified Pin 36	V_{36}		1.5		V
SECAM reference output dc voltage	SECAM forced or identified Pin 36	V_{36}		4.4		V
SECAM reference frequency	Pin 36	f_{ref}		4.43		MHz
Required current (from U4935B) to stop PAL/ NTSC identification	SECAM identified by U4935B Pin 36	I_{36}	120	180		A
Chrominance processing						
Chroma bandpass filter center frequency	Correction OFF Correction ON	f		fsc fsc+0.3		MHz
ACC control range		ΔACC	26			dB
Change in amplitude of –(R–Y), –(B–Y)-signals over ACC control range	Variable C (SVHS) +6/–20 dB Pins 39, 40	ΔG			3	dB
C (SVHS) input level at killer ON	Related to nom. input Pins 21, 22, 23	v_i		–45	–40	dB
Color remaining at killer ON	Pins 21, 22, 23	v_o			20	mV
Oscillator catching range (fsc = 4.43 and 3.58 MHz)	Referred to the free running frequency f_{sc}	Δf	±300	±600		Hz
Tint control range (0 to 127 steps)	NTSC-signal	ϕ		45		°

Electrical Characteristics (continued)

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
RGB processing – Inputs						
–(R–Y) input signal (peak-to-peak value)	All standards (SECAM with U4935B) Pin 32	v_{32}		1.05		V
–(R–Y) clamping level	Pin 32	V_{32}		3.0		V
–(R–Y) input impedance	Pin 32	Z_{32}	1			MΩ
–(B–Y) input signal (peak-to-peak value)	All standards (SECAM with U4935B) Pin 31	v_{31}		1.33		V
–(B–Y) clamping level	Pin 31	V_{31}		3.0		V
–(B–Y) input impedance	Pin 31	Z_{31}	1			MΩ
RGB insertion input signals (peak-to-peak value)	For an output signal of 2 V (black-to-white) Pins 27, 28, 29	$v_{27,28,29}$		0.7		V
RGB insertion clamping level	Pins 27, 28, 29	$V_{27,28,29}$		2.6		V
RGB insertion input impedance	Pins 27, 28, 29	$Z_{27,28,29}$	1			MΩ
Insertion switch input voltage for no data insertion	Pin 30	V_{30}			0.3	V
Insertion switch input voltage for data insertion	Pin 30	V_{30}	0.9		3.0	V
Insertion switch input voltage for OSD	Note 2 Pin 30	V_{30}	4.0		5.0	V
RGB processing						
Saturation control curve	See figure 5					
Saturation control range (step 1 to 127)	Pins 21, 22, 23	$G_{sat.}$		22		dB
Saturation attenuation (step 0 to 127)	Pins 21, 22, 23	$G_{sat.}$		50		dB
Contrast control curve	See figure 6					
Contrast control range (step 0 to 127)	Pins 21, 22, 23	$G_{contr.}$		35		dB
Brightness control curve	See figure 7					
Brightness control range (step 0 to 127)	Pins 21, 22, 23	$V_{21,22,23}$		2		V
R, B – drive control range (step 0 to 63)	Pins 21, 23	$G_{21,23}$		6.0		dB
RGB cut off control curve	See figure 8					
RGB cut off control range (step 0 to 255)	Pins 21, 22, 23	$V_{21,22,23}$	1.7	2.0	2.3	V
RGB output signal ratio between V(Pin 25) = 3.6 V and V(Pin 25) = 2.2 V (Beam current limiting)	Pins 21, 22, 23	G_{25}		–26		dB

Electrical Characteristics (continued)

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
RGB processing – Outputs						
RGB output signals (peak-to-peak value)	Pins 21, 22, 23	$v_{21,22,23}$	1.7	2.0	2.3	V
Max. RGB output signals (peak-to-peak value)	Contrast max Pins 21, 22, 23	$v_{21,22,23}$	3.0	3.4		V
RGB output black level	Pins 21, 22, 23	$V_{21,22,23}$	2.6	3.0	3.4	V
Black level difference R–G	Pins 21, 22	$V_{oR}-V_{oG}$	–100	0	+100	mV
Black level difference G–B	Pins 22, 23	$V_{oG}-V_{oB}$	–100	0	+100	mV
Black level difference R–B	Pins 21, 23	$V_{oR}-V_{oB}$	–100	0	+100	mV
RGB output frequency characteristic from CVBS-1, CVBS-2 CVBS-1, CVBS-2, Y(SVHS) –(R–Y), –(B–Y) input RGB insertion inputs	3 dB bandwidth Pins 21, 22, 23 with 4.43 MHz trap with 3.58 MHz trap without trap	f_{BW}		 3.1 2.6 8 4 10		 MHz
Horizontal deflection						
Minimal current during sync pulse	No sync input signal Note 3 Pin 52	I_{52min}		–0.1		mA
Horizontal free running frequency	No sync input signal Pin 7	f_{osc}		15.7		kHz
Horizontal catching range	Pin 7	f		350		Hz
PHI1 time constant change	Note 4 Pin 9			7.5		dB
Sandcastle pulse level during vertical blanking	Pin 4	V_4		1.6		V
Sandcastle pulse level during horizontal blanking	Pin 4	V_4		2.9		V
Sandcastle pulse level during BGP	Pin 4	V_4		4.5		V
Burst gate pulse (BGP) position	Time difference between the beginning of BGP and the end of sync pulse Pin 4	t_1		2		µs
BGP width	Pin 4	t_w		6		µs
Horizontal pulse level	Pin 6	V_{oH}		4.0		V
Horizontal pulse position	Time between the start of the horizontal out and the beginning of the sync pulse (Pin 52) Pin 6	t_2		8.5		µs
Horizontal pulse width	Pin 6	t_w		26		µs

Electrical Characteristics (continued)

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Horizontal processing						
Horizontal stop function	HPD = 1 Pin 6	V_o		4.0		V
Horizontal shift range	Hshift = max, min Pin 6	t_{Hsh}		1.5		µs
Vertical deflection						
Reference voltage	Pin 12	V_{ref}		4		V
Vertical oscillator free running frequency – search – forced 50 Hz – forced 60 Hz	No sync input signal Pin 14	f_o		 44 48 55		 Hz Hz Hz
Vertical oscillator locking range	Pin 14	n_l	233		352.5	lines/ field
Vertical drive out common mode current	Pins 13, 14	$I_{13,14}$		–200		µA
Vertical drive out amplitude	Pins 13, 14	$\Delta I_{13,14}$		± 75		µA
Vertical processing						
Vertical slope control curve	See figure 9					
Vertical slope control range	Vslope = max, min Pin 11	ΔV_{11}		± 15		%
Vertical size control curve	See figure 10					
Vertical size control range	Vsize = max, min Pins 13, 14	$\Delta V_{13,14}$		± 20		%
S-correction control curve	See figure 11					
S-correction control range	Scorr. = max, min Pins 13, 14	$\Delta V_{13,1}4$		± 15		%
Vertical shift control curve	See figure 12					
Vertical shift control range	Vshift = max, min Pins 13, 14	$\Delta V_{13,14}$		± 5		%
Vertical amplitude reduction for compressed mode	COMP = 1 Pins 13, 14	$\Delta V_{13,14}$		25		%

Notes

1. e.g.: R output level ratio = 20 × log [$v_{R\ (VMUTE(ON))}$ / $v_{R\ (VMUTE(OFF))}$] [dB]
2. Required input voltage to insert ”black level” at the RGB outputs, so that OSD (on screen display) signals can be added to the outputs
3. Measure the current at Pin 52 for a vertical period at Pin 11 of 233 lines per field
4. Measure the Pin 9 output current peak-to-peak amplitude
   PHI1 time constant change = 20 × log [i_{PHI1T}= 0 / $_{iPHI1T}$= 1] [dB]

Control Ranges of Luminance, Chrominance and R/G/B Processing

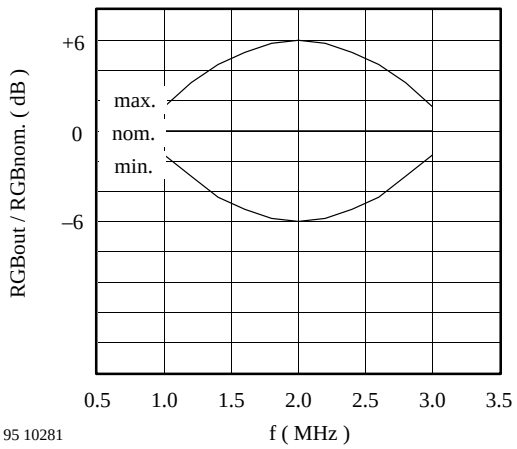


Figure 4. Sharpness control range

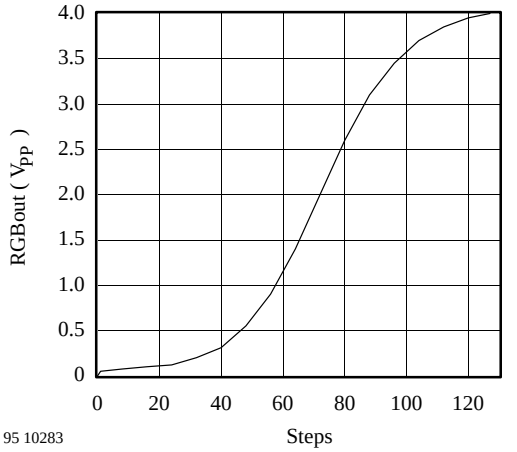


Figure 5. Saturation control range

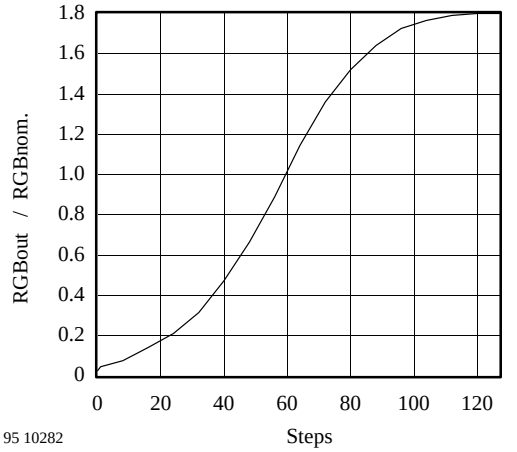


Figure 6. Contrast control range

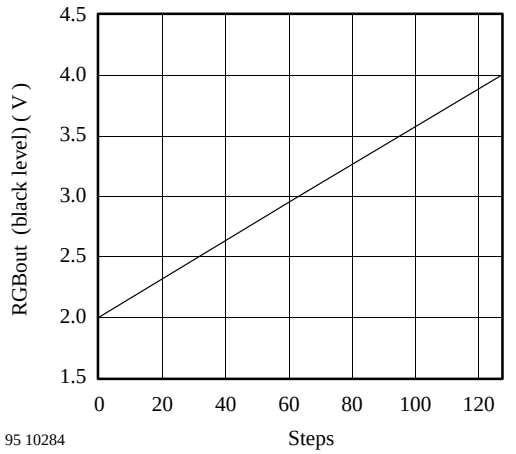


Figure 7. Brightness control range

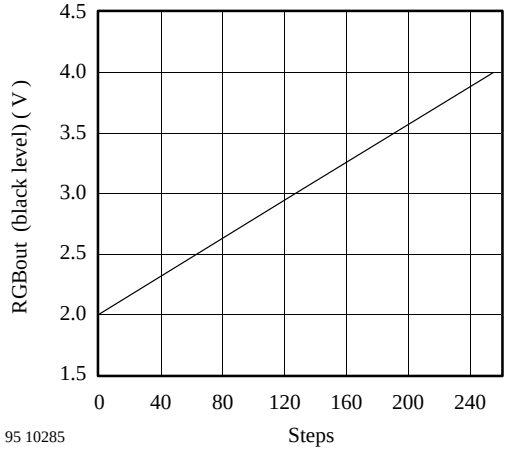


Figure 8. Cut-off control range

Control Ranges of Deflection

Note: T = 1 vertical period

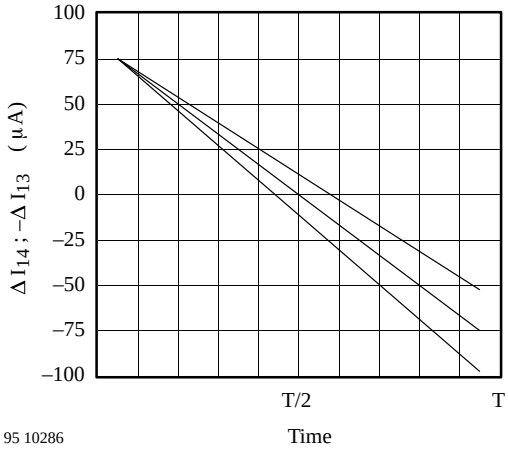


Figure 9. Vertical slope control range

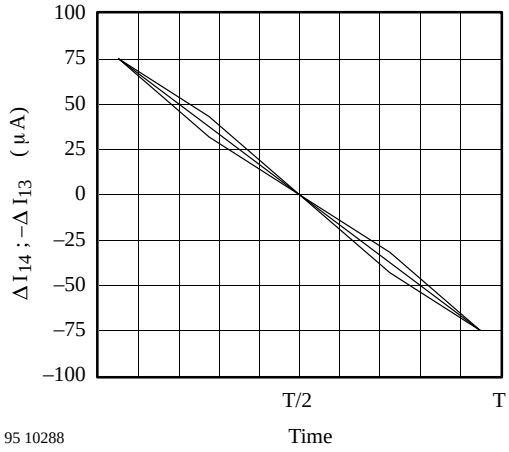


Figure 11. S-correction control range

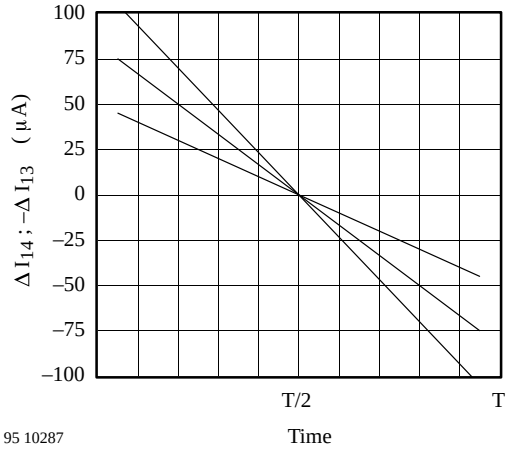


Figure 10. Vertical size control range

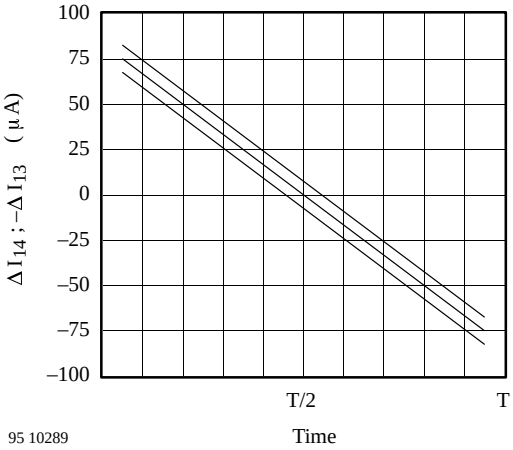


Figure 12. Vertical shift control range

Internal Pin Configuration

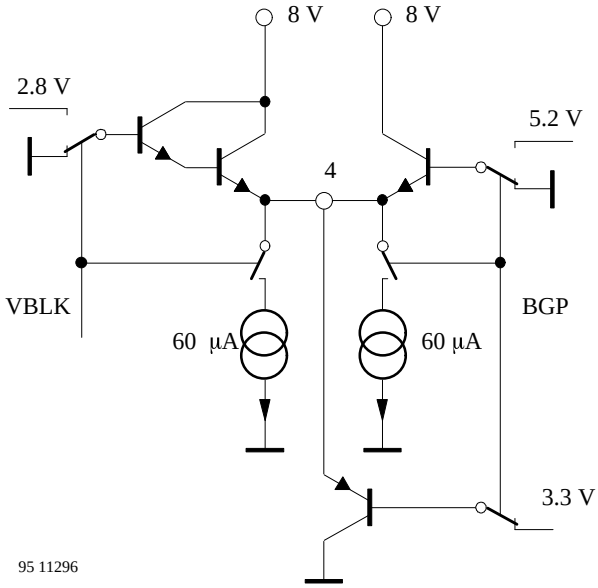


Figure 13. Sandcastle-pulse output

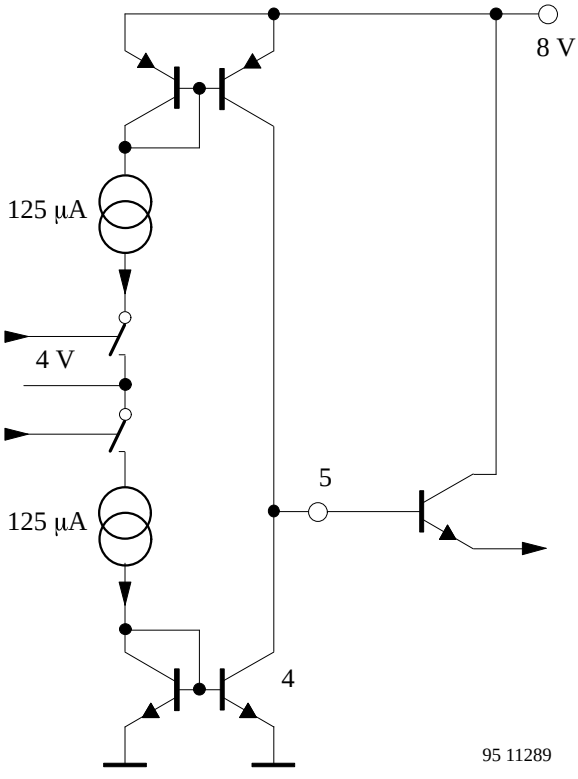


Figure 14. Mute output

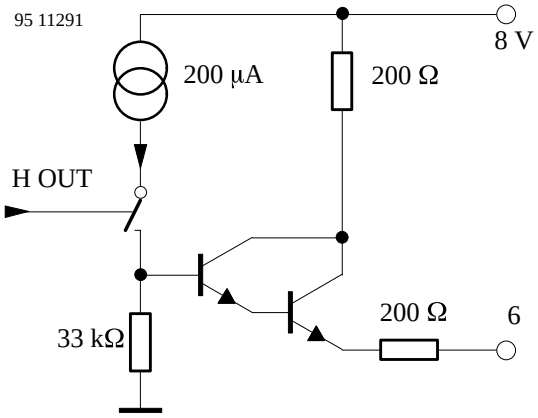


Figure 15. Horizontal output

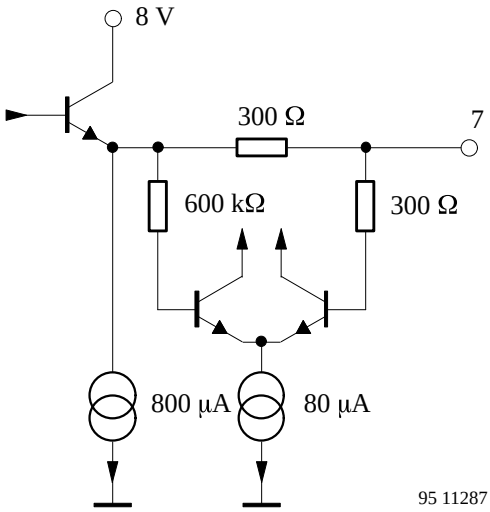


Figure 16. Horizontal oscillator

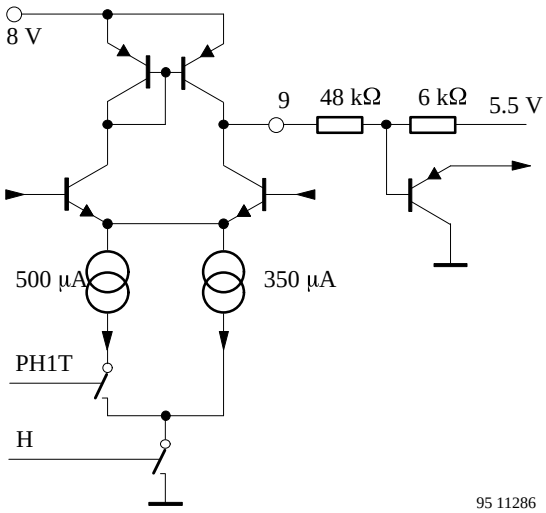


Figure 17. PHI1 loop filter

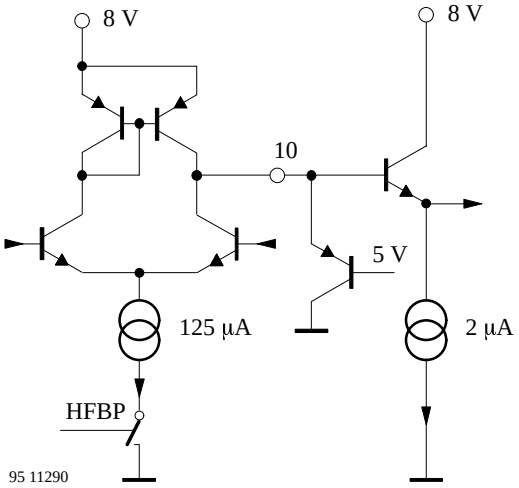


Figure 18. PHI2 loop filter

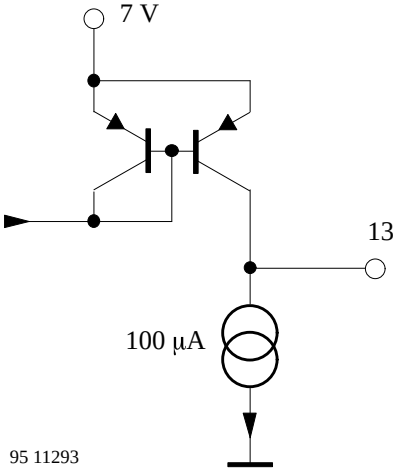


Figure 21. Vertical drive (positive)

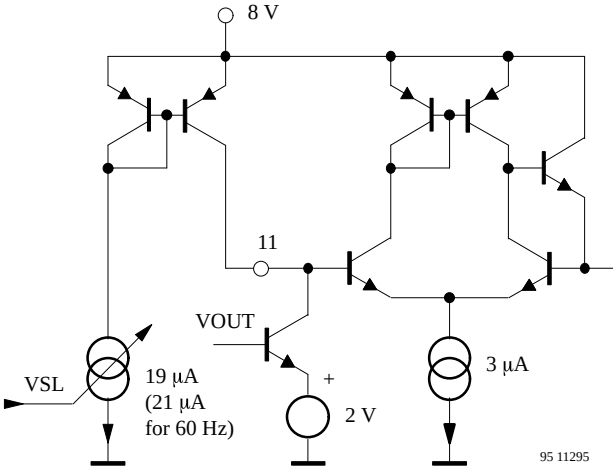


Figure 19. Vertical sawtooth capacitor

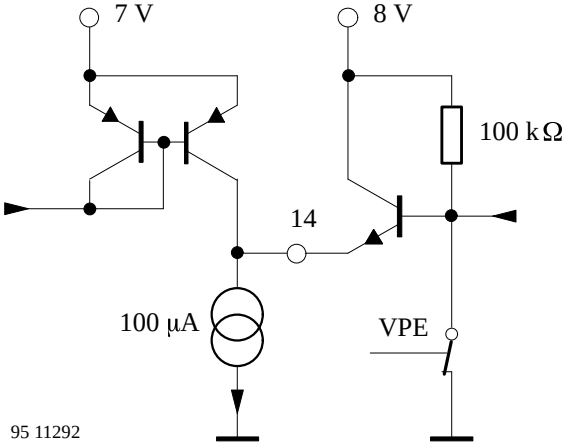


Figure 22. Vertical drive (negative)/vertical pulse

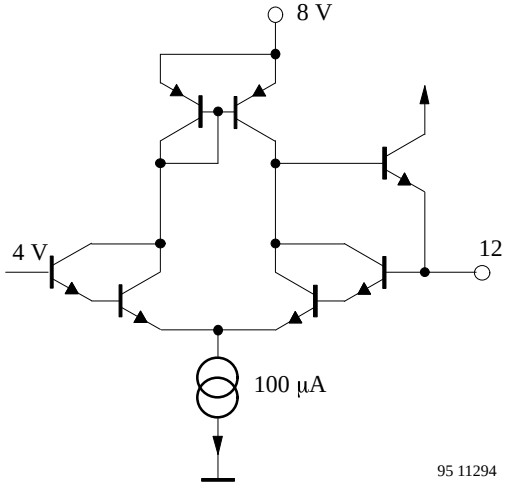


Figure 20. Reference current (Iref)

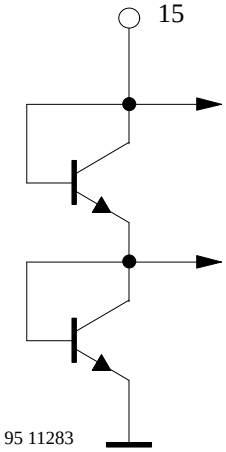


Figure 23. Vs (digital)

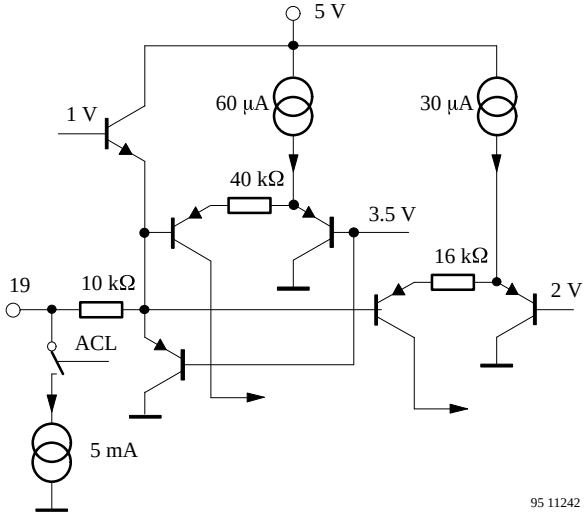


Figure 24. ACL filter

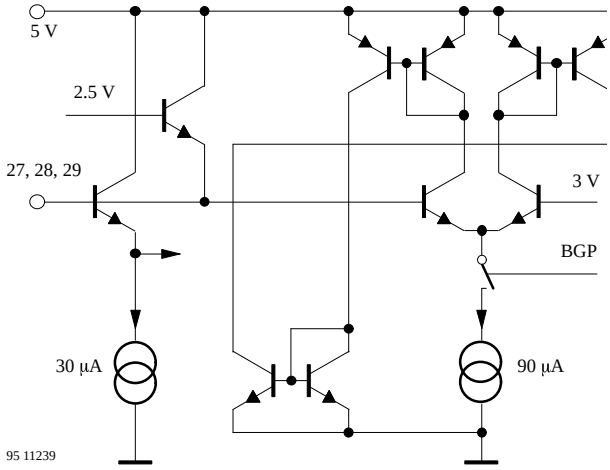


Figure 27. B/G/R input

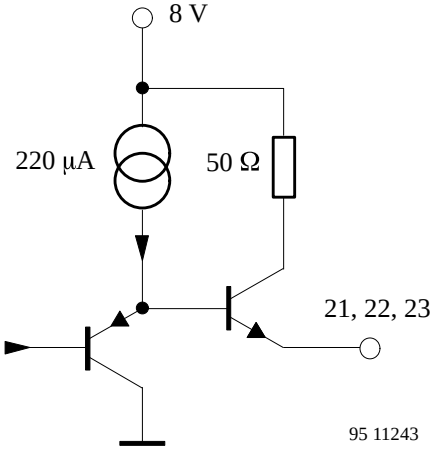


Figure 25. R/G/B output

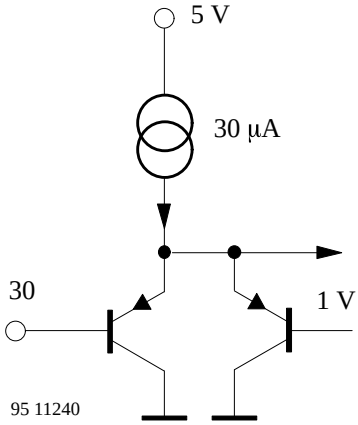


Figure 28. Insertion switch

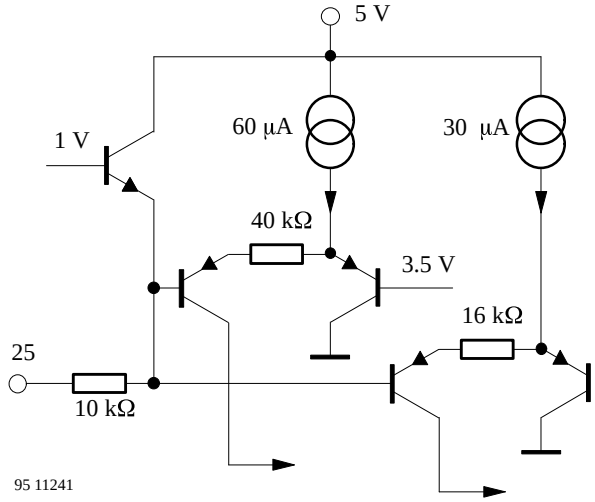


Figure 26. BCL input

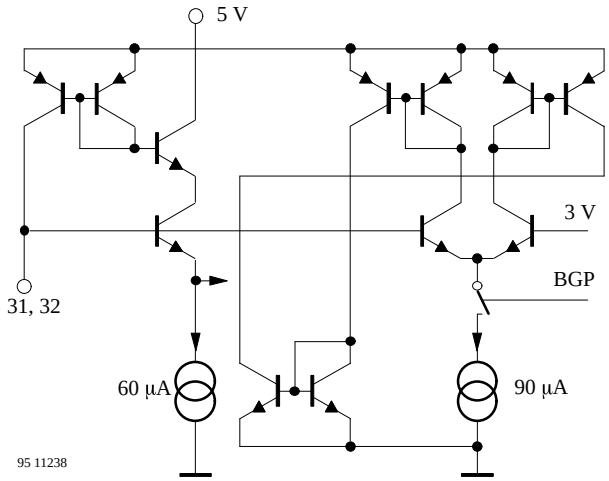


Figure 29. –(B-Y)/–(R–Y) input

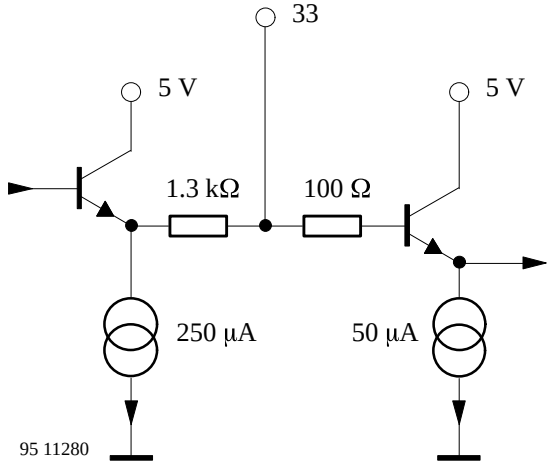


Figure 30. Crystal 4.43 MHz

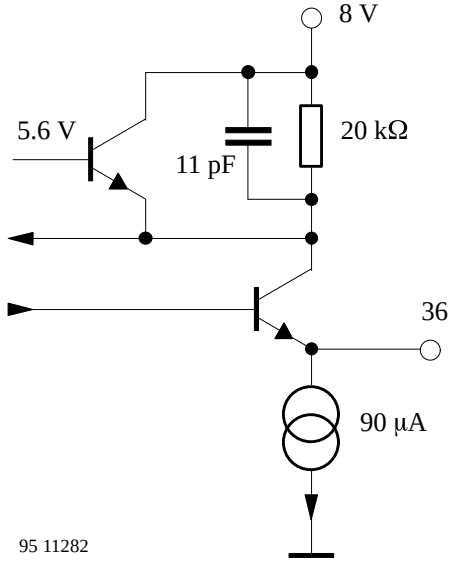


Figure 33. SECAM reference output

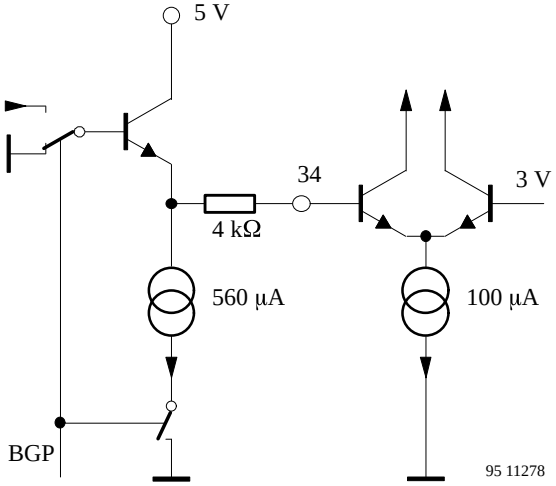


Figure 31. APC filter

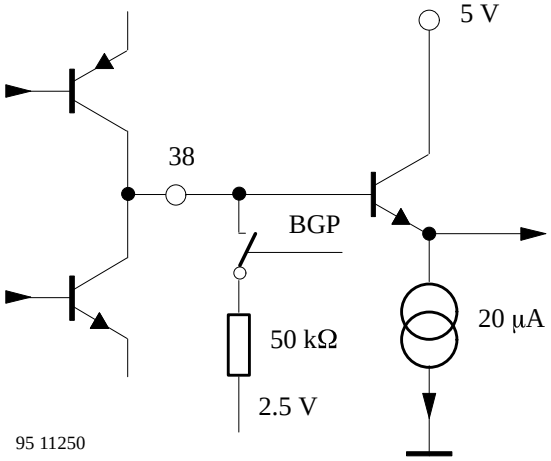


Figure 34. Ident filter (frequency)

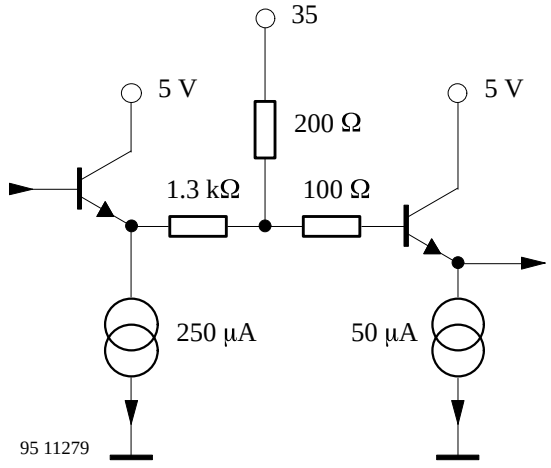


Figure 32. Crystal 3.58 MHz

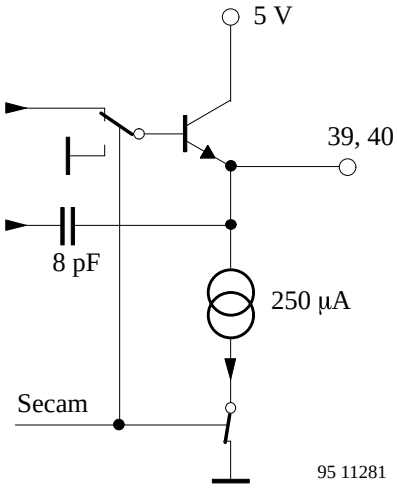


Figure 35. –(R-Y)/–(B–Y) output

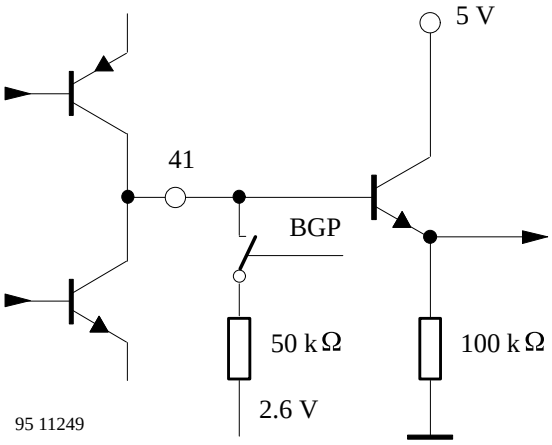


Figure 36. Ident filter (PAL phase)

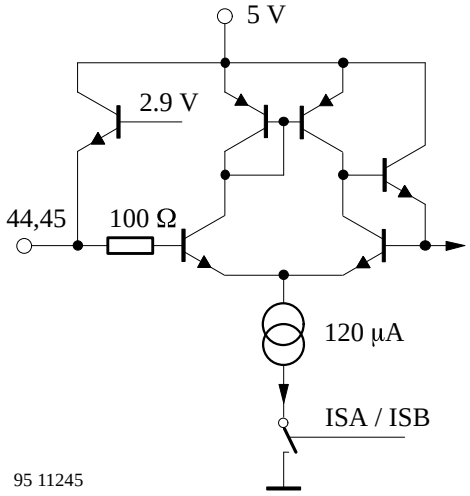


Figure 39. CVBS-1/CVBS-2 input

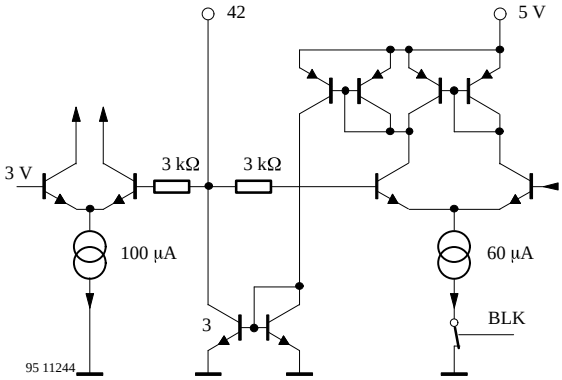


Figure 37. Black peak hold

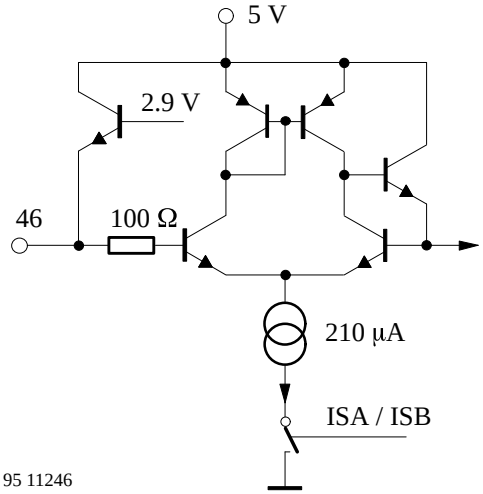


Figure 40. Y(SVHS) input

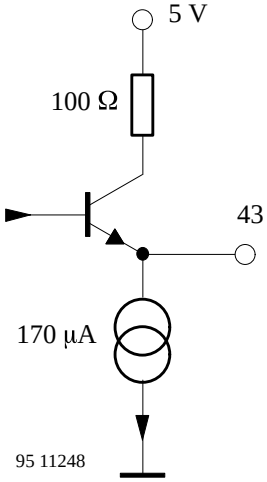


Figure 38. CVBS-SCART output

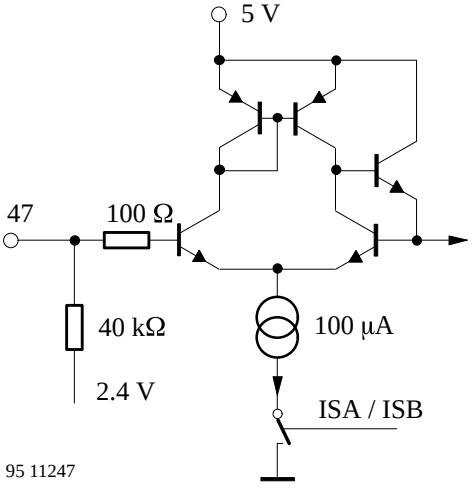


Figure 41. C(SVHS) input

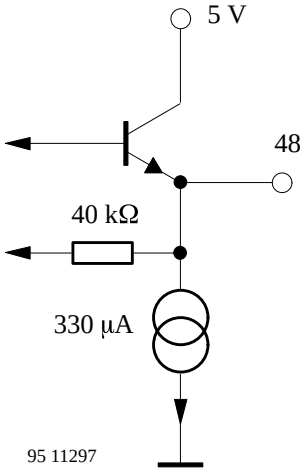


Figure 42. CVBS-TXT output

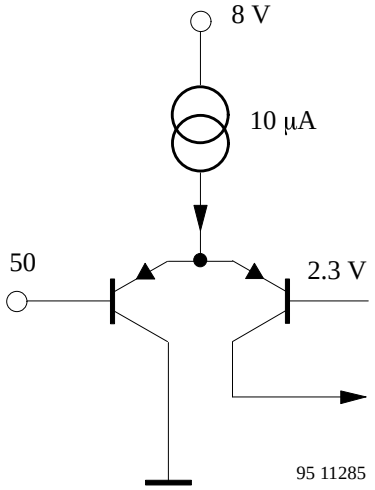


Figure 44. SCL (I^2C-Bus)

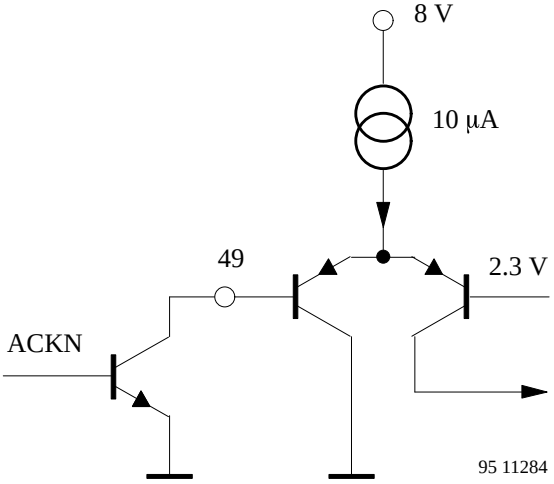


Figure 43. SDA (I^2C–Bus)

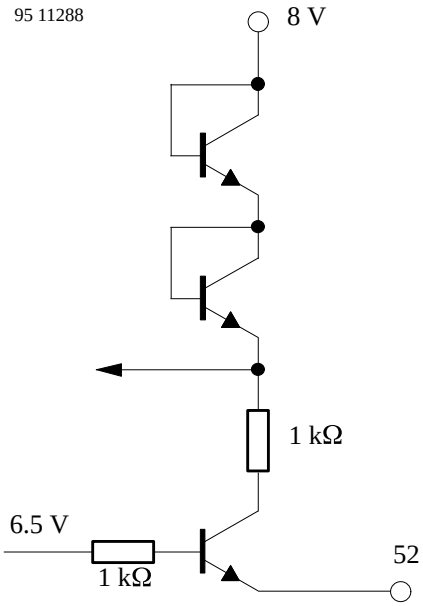


Figure 45. Sync separation input

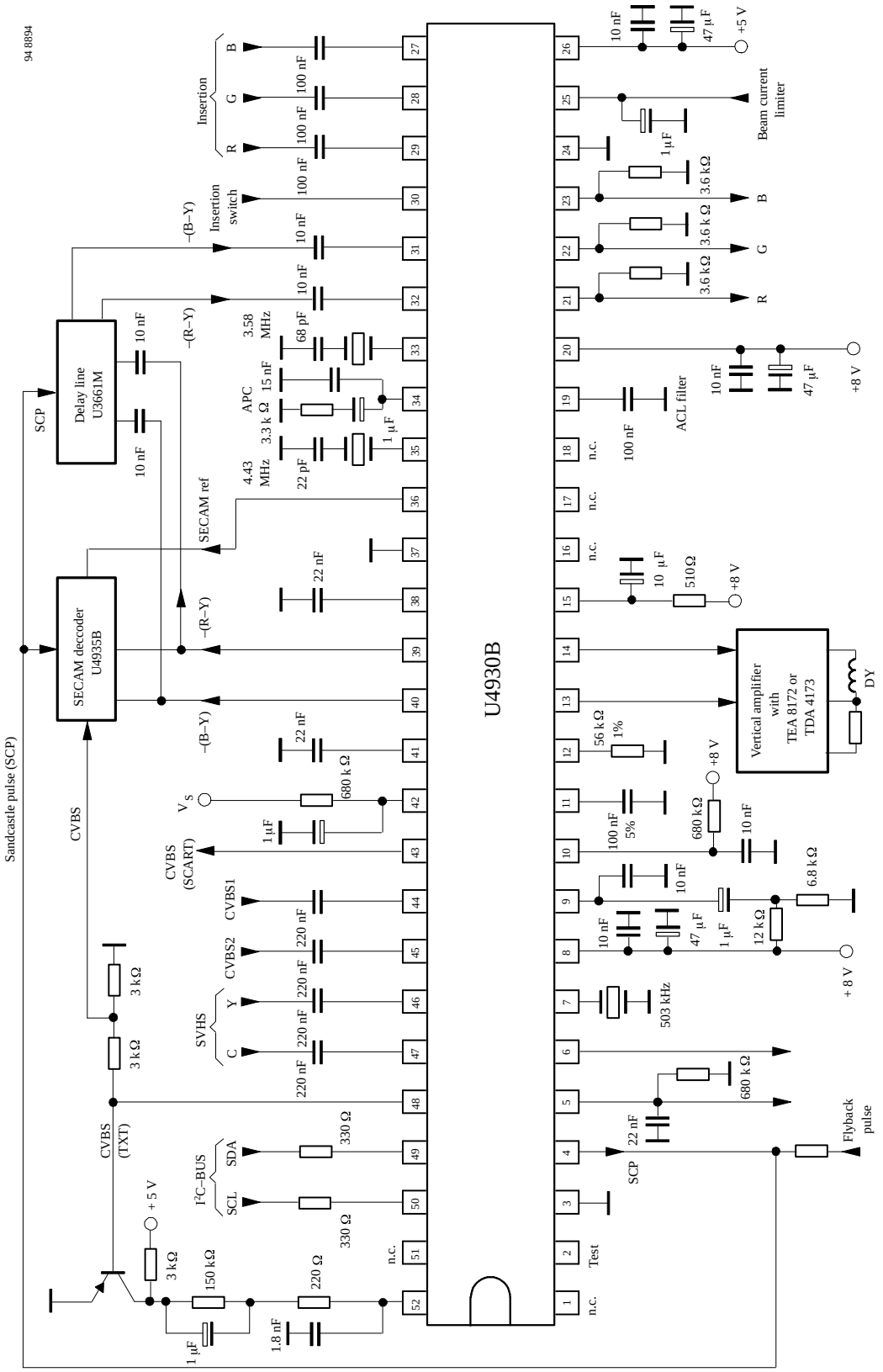
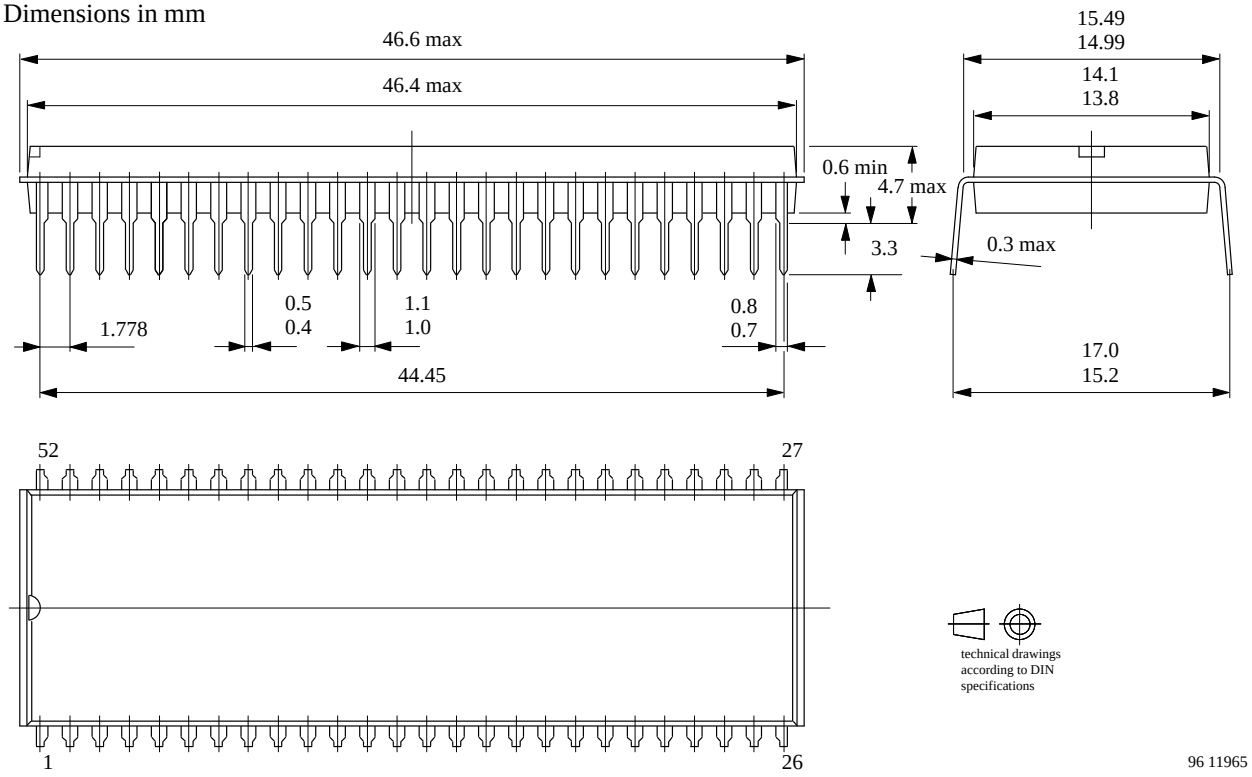


Figure 46. Basic application circuit

Package Information

Package SDIP52
Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC TELEFUNKEN microelectronic GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC TELEFUNKEN microelectronic GmbH semiconductor division has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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